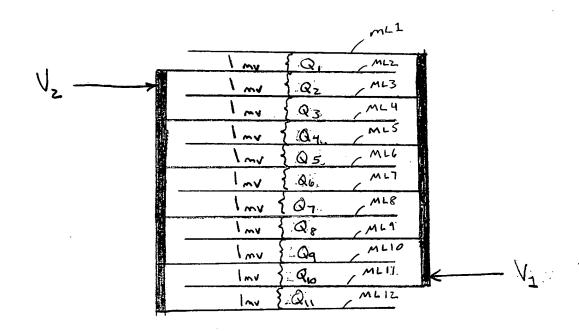
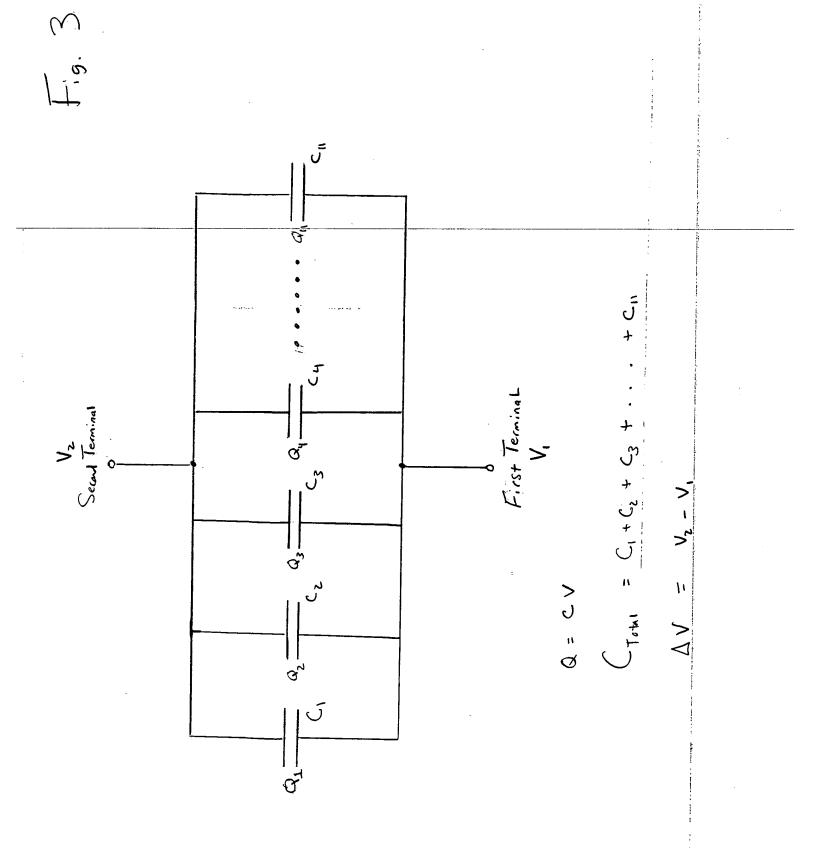
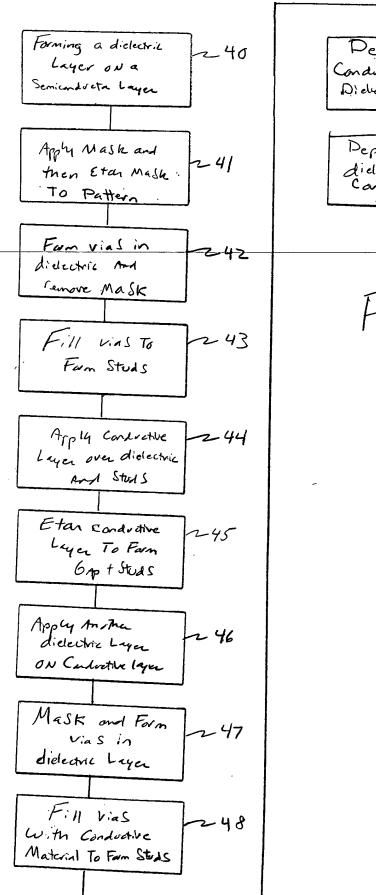


Fig. 1







Deposit Another
Conductive Layer over
Dichectore Layer

Deposit Additional
dicloctore and
Conductive Layers
As needed

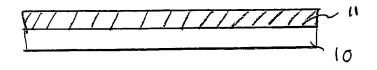


Fig. Sa)

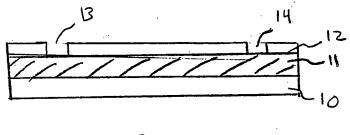
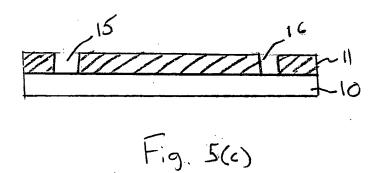
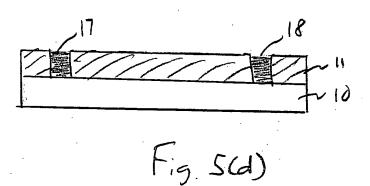
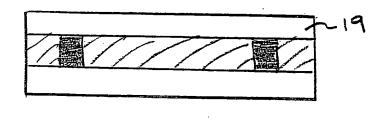
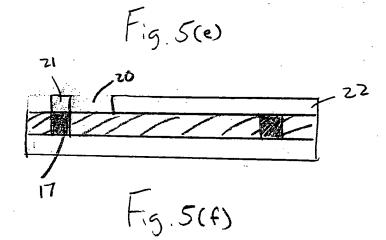


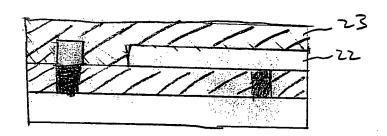
Fig. 5(b)











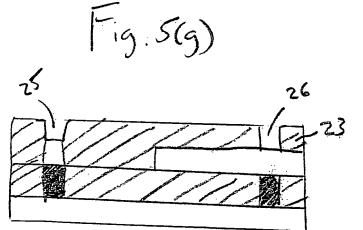


Fig. 5(h)

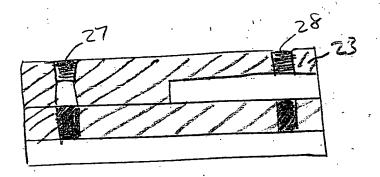


Fig. 5(1)

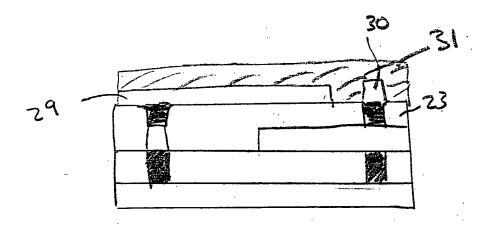
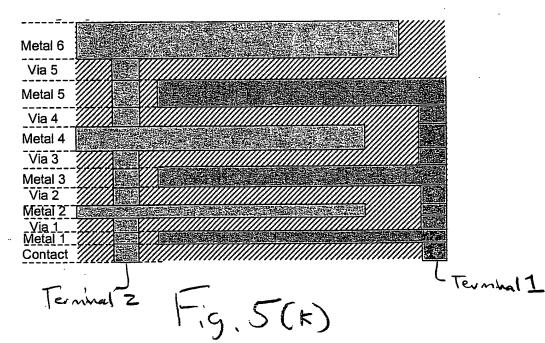


Fig. 5(i)



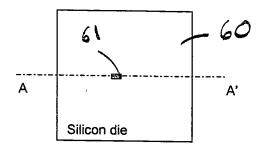


Fig.6(a)

## **Equivalent capacitor**

Fig.6(6)

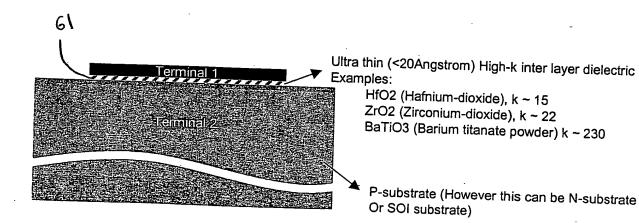


Fig. 6(1)

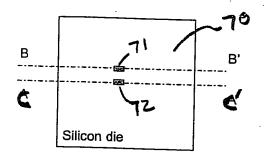
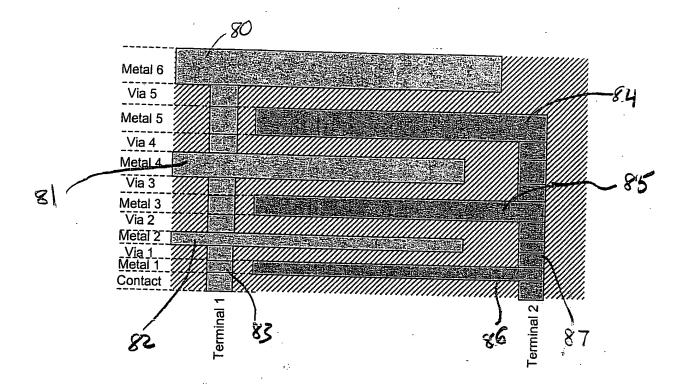


Fig.7(a)

Fig.7(b)



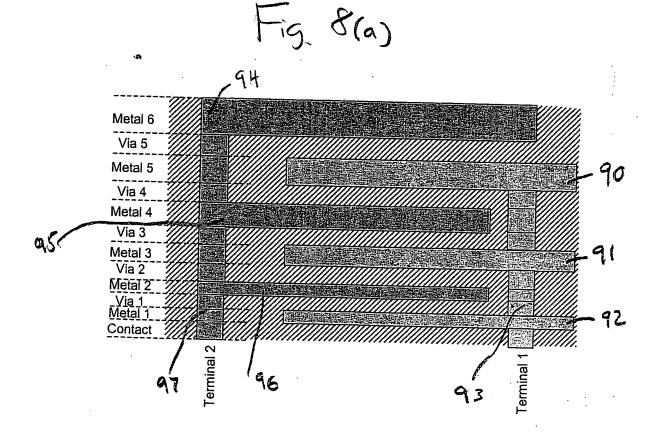


Fig. 8(b)

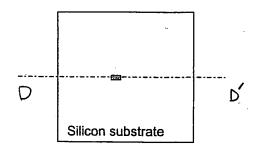


Fig. 9(a)

## **Equivalent capacitor**

Terminal 1
$$C_{oc_1} = V_1$$

$$C_{oc_2} = V_2$$
Terminal x
$$V_2$$
Terminal 2

Fig. 9(b)

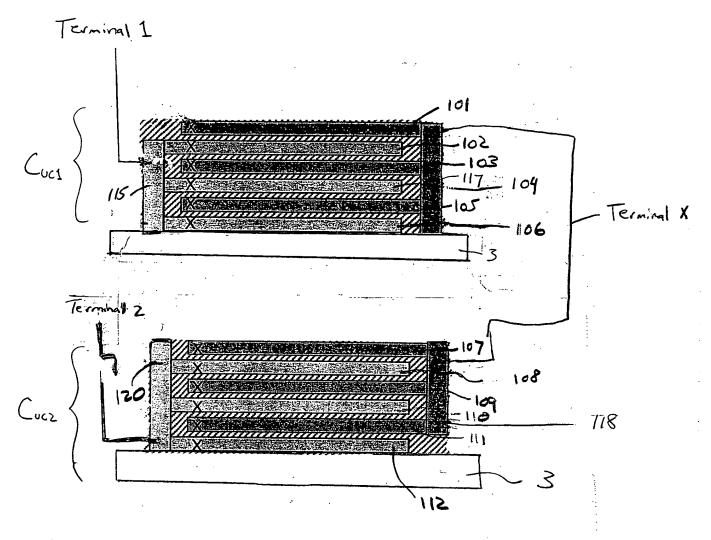
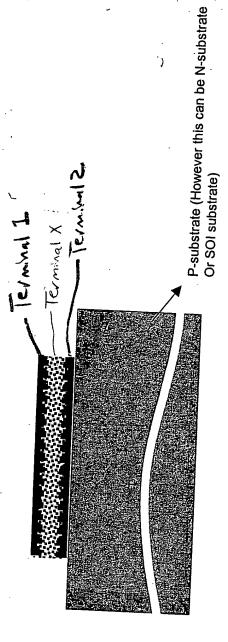


Fig. 10



Electrode (Terminal 1) – Example: Porous carbon or doped silicon. Can be conductive carbon or silicon nanotube. Electrolyte (Terminal x) – Example: Potassium hydroxide Electrode (Terminal 2) – Example: Porous carbon or doped silicon. Can be conductive carbon or silicon nanotube.

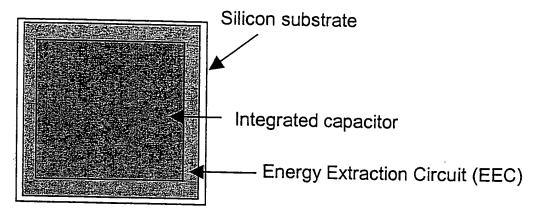
Example cross section showing stacking of multiple substrate to increase the capacitance per unit area

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	SANCE SANCE									
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	APERE THE PERE	CORE C								9 25
	12:368 12:368 15:363 16:363 16:363									
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Terminal 1

7.6.1

## **Energy Extraction Circuit (Integrated with the capacitor)**



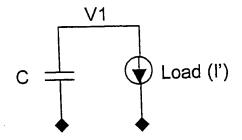


Fig. 14

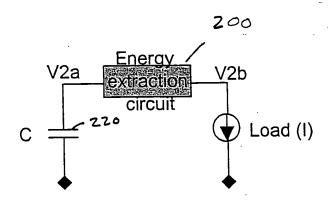
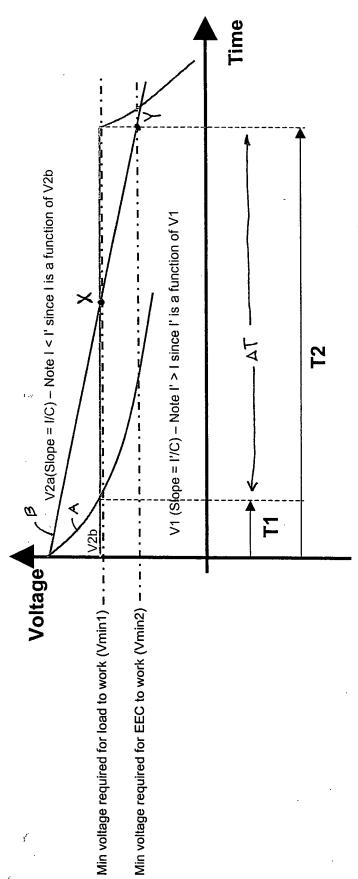


Fig. 16



T2 - Duration for which the capacitor energy can be used by the load with EEC T1 - Duration for which the capacitor energy can be used by load without EEC

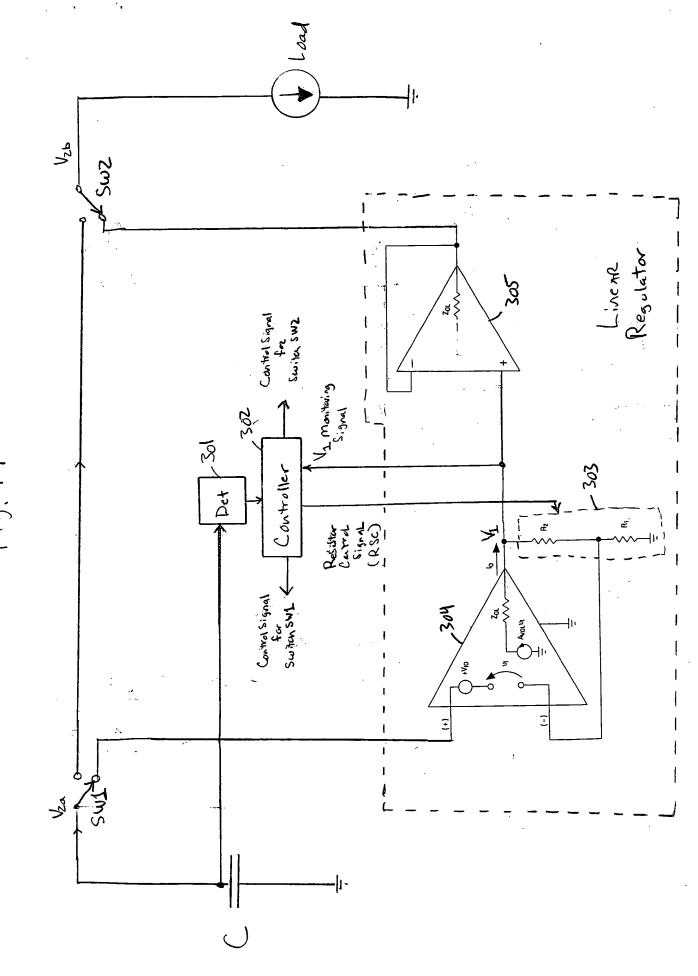
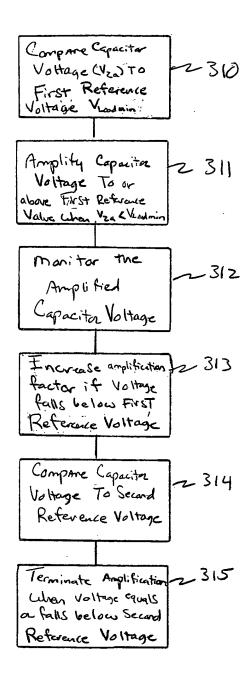
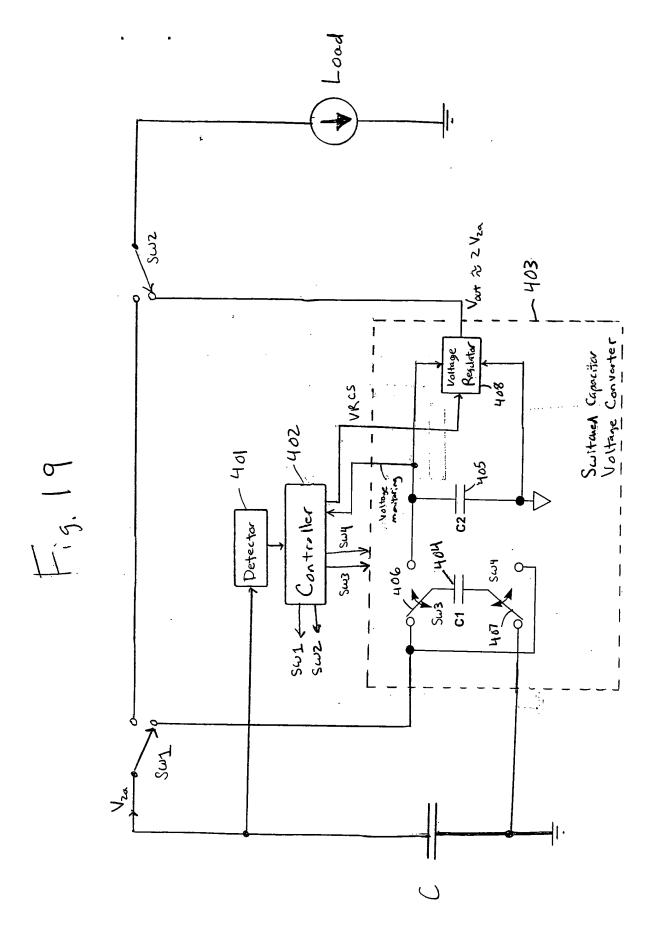
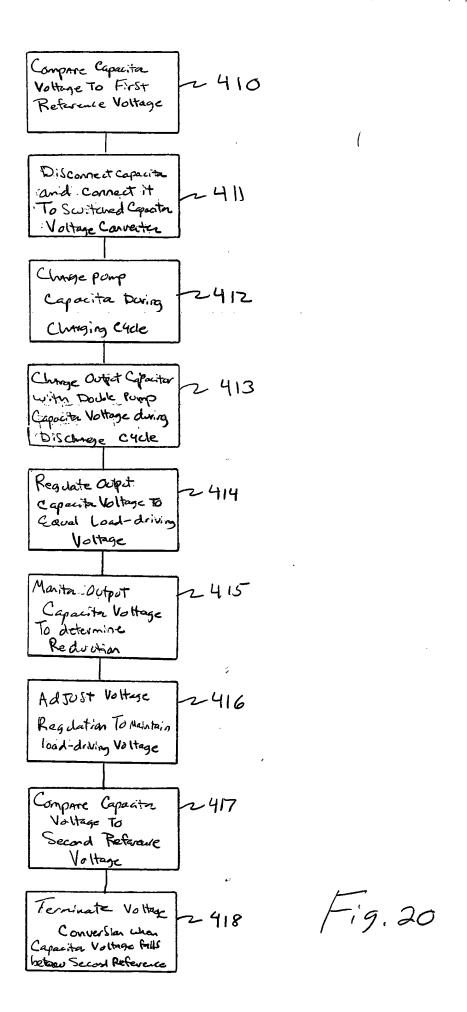


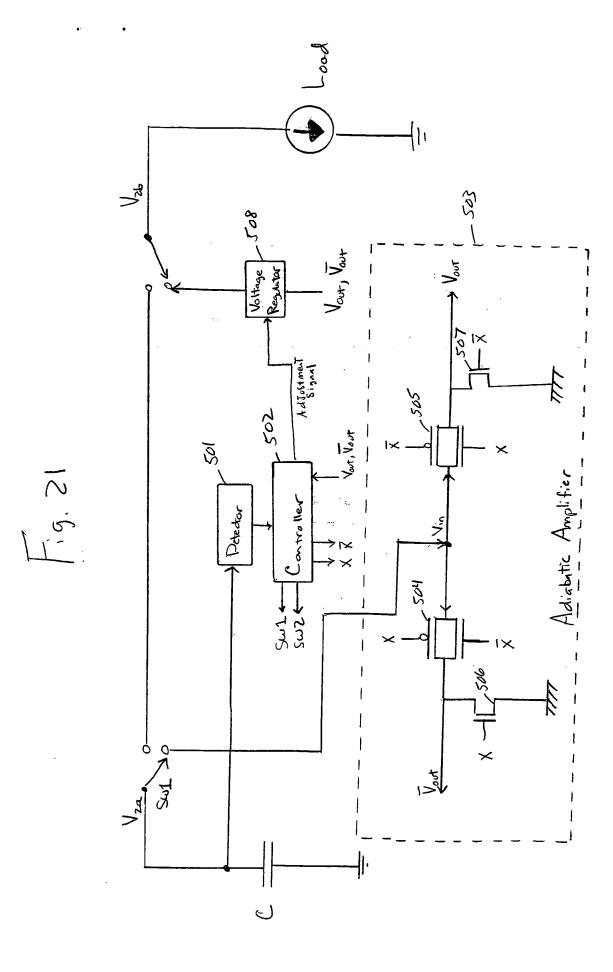
Fig. 17







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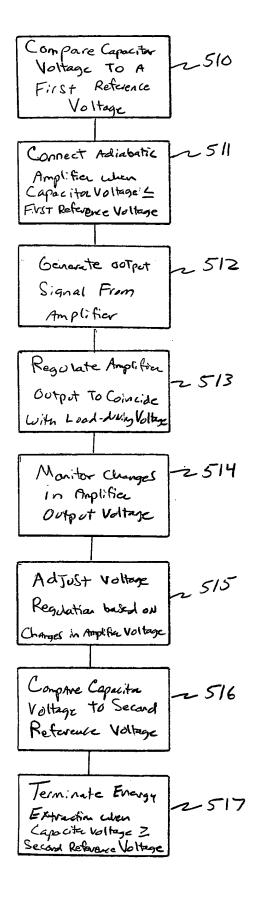


Fig. 22

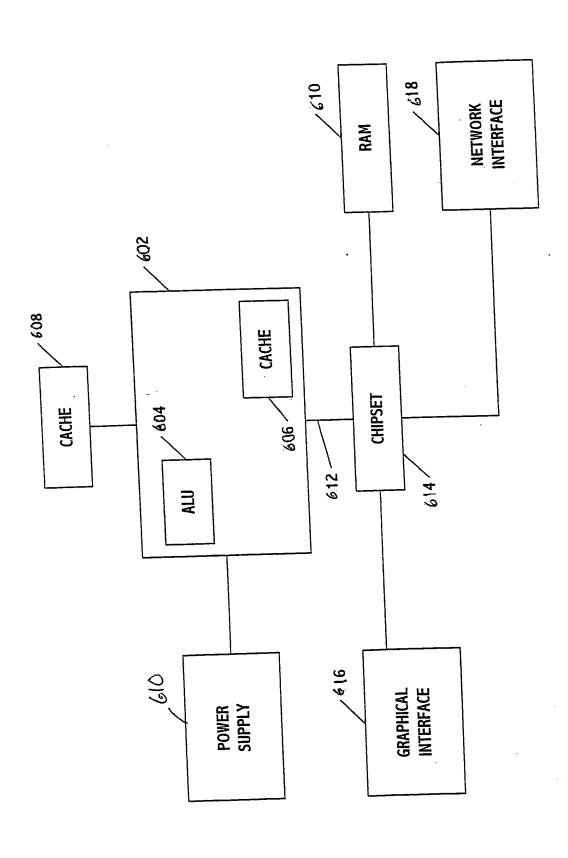


FIG. 23